

The Grand Challenges in Microelectronics Design



μ GC4: Building Brains – Brain Inspired Electronic Systems

19th Sept 2008, Edinburgh International Conference Centre

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The workshop will run on 19th Sept as part of the ESSDERC conference and is supported by the EU Network of Excellence NANOSIL, Visionary Project 2.5.1 and the UK Design Vision: 'Grand Challenges in Microelectronic Design – μ GC4 Building Brains

Objectives

The objective of this Grand Challenge is to create microelectronic designs and architectures that deliver very high levels of performance for this area, and thereby help test hypotheses and explore the wider space of asynchronous event-coupled dynamic systems. Progress towards this Grand Challenge would create systems enabling much larger neural models to be simulated than is possible at present. This is likely to be a significant contribution to the higher-level understanding of the architecture of brain and mind, whose impact upon humanity would be dramatic.

Agenda:

9:00: **Introduction and overview "Building Brains"**: Wayne Luk, Imperial College, UK and Daniel Dearing, Knowledge Transfer Network, UK.

10:00 **Coffee, Posters and Networking** – *Interested delegates are encouraged to contribute a poster to promote their research*

10:45 **Giacomo Indiveri**, ETHZ, Switzerland.

11:15 **Piotr Dudek**, University of Manchester, UK.

11:55 **Leena Patel/Alan Murray**, University of Edinburgh, UK.

12:15 **Networking Lunch**

13:30 **Alex Rast**, University of Manchester, UK.

14:00 **Steve Hall/Liam McDaid**, University of Liverpool/ University of Ulster, UK.

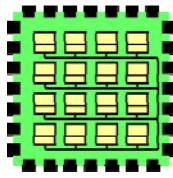
14:30 **Workshop Breakout Session**, facilitated by partner organisations and aimed at identifying themes and research projects including those of use to industry

15:30 **Feedback Session and Discussion**, nominated speakers from each of the workgroups present the outcomes, followed by open discussion.

16:00 Coffee

16:15 **Daniel Dearing, eKTN** – Summary and follow-up

16:30 **Networking & Close**



BIES: Brain-Inspired Electronic Systems

Significant research has focused on the development of Neural Networks (NNs) models that can be implemented in hardware and used to inspire new techniques for real time computations. However, there exist several fundamental bottlenecks that restrict the progress towards biological scale networks in hardware: power consumption, compactness of neuron cells and interconnect, off vs. on chip training and many others.

The aims of this workshop are to present and discuss recent advances in this area, to provide a networking opportunity for bringing together researchers to discuss issues related to the development of novel hardware platforms for Brain-Inspired Electronic Systems and to consider routes to consolidating research activity. The day will include a number of presentations and also breakout sessions to explore collaborations and associated funding opportunities.

Delegates from both academia and industry are most welcome.

The workshop will provide an opportunity for researchers focusing on various aspects of such systems, such as hardware implementation of spiking neurons and the associated networks, to discuss and compare different approaches to the realization of large-scale platforms. In particular, we would like the session to draw on the expertise of researchers to provide a discussion platform on many issues related to this domain. Also the workshop will provide an opportunity to discuss applications of Brain-Inspired Electronic Systems: for example fault tolerant computational systems.