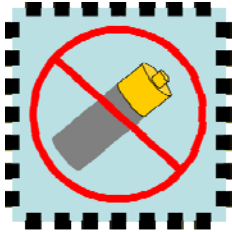


The Grand Challenges in Microelectronics Design



μ GC1: Batteries Not Included – Minimising the Energy Demands of Electronics

July 16th, Millbrook Technology Campus, Southampton.



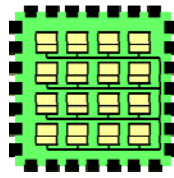
Objectives

The objective of this Grand Challenge is to develop advances in technology and design that significantly decrease the energy requirements of electronic devices, in particular mobile digital devices. This will be based around the development of design techniques to address the increasingly unreliable aspects of the transistors and to explore the possibilities of self-powered electronics to develop systems that do not need regular user attention to battery charging or replacement. We take the modern wristwatch as an exemplar, which delivers many years of operational life from a single battery, in some cases operating from scavenged energy such as solar or kinetic power.

Agenda:

- 9:00 Registration
- 9:30 **Professor Bashir Al-Hashimi** – Introduction to the Batteries Not Included Theme
- 9:45 **Prof. Asen Asenov, Glasgow Uni.** "Statistical CMOS variability and its impact on low power design."
- 10:15 **Dr. George Constantinides, Imperial College** "Low Power Design for Reconfigurable Computing".
- 10:45 **Dr. Steve Beeby, Southampton Uni.** 'Vibration Energy Harvesting: Background and state of the art'
- 11:15 Coffee Break
- 11:45 **Prof. Roger Woods, Queens Uni. Belfast** "The need to mix programmability and low power"
- 12:15 **Prof. Alex Yakovlev, Newcastle Uni.,** "From low power computing to power-adaptive computing"
- 12:45 Networking Lunch
- 14:00 **Robin Sharpe, Director of Strategy and Technology – NXP Semiconductors,** "Priorities for Low Power"
- 14:30 **Workshop Session** – facilitated by partner organisations and aimed at identifying academic research projects that might be of use to industry
- 15:30 Coffee
- 16:00 **Feedback Session** – nominated speakers report the outcomes of each workshop group
- 16:15 **Daniel Dearing, eKTN** – Summary and follow-up

Register here: http://www.regonline.co.uk/batteries_not_included



16:30 Networking and close

Presentation Abstracts

Asen Asenov, Glasgow Uni. "Statistical CMOS variability and its impact on low power design."

Statistical variability introduced by discreteness of charge and granularity of matter which cannot be reduced by better process control, has become a major concern associated with CMOS transistors scaling and integration. It already critically affects SRAM scaling, and introduces leakage and timing issues in digital logic circuits. The variability is the main factor restricting the scaling of the supply voltage, which for the last three technology generations has remained constant, adding to the looming power crisis. Therefore, it is very important to understand properly how the variability will affect the low power design and the scaling of the supply voltage in the future technology generations.

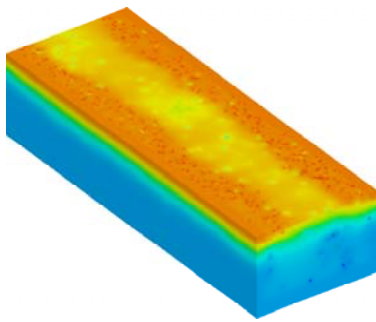


Fig. 1 Random discrete dopants in combination with line edge roughness in a 35 nm MOSFET from the present 90 nm technology node.

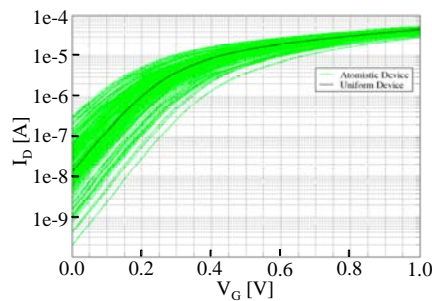


Fig. 2 Random dopant induced variations in the current-voltage characteristics of 200 13 nm transistors with different dopant distributions.

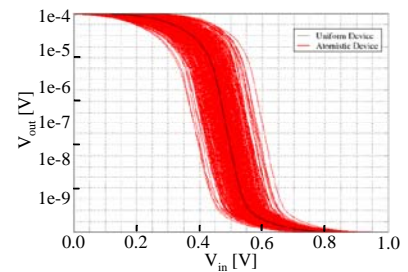
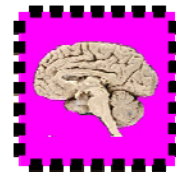
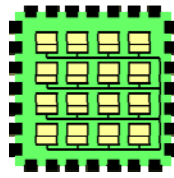


Fig. 3 Random dopant induced variations in the transfer characteristics of inverters made of 13 nm transistors.

In this talk we review the major sources of variability in CMOS devices focusing at and beyond 45nm technology generation and beyond. We examine intrinsic parameter fluctuations introduced by discreteness of charge and matter, which play an increasingly important role in the present and future CMOS devices and cannot be controlled or reduced by tightening the process tolerances. Among the most important sources of intrinsic parameter fluctuations are the random discrete dopants in combination with line edge roughness illustrated in Fig. 1, which makes every transistor microscopically different from its counterparts and introduces differences in the characteristics of topologically identical devices (Fig. 2). The corresponding parameter variations introduce significant variation in the operation of the major digital building block, the inverter illustrated in Fig. (3). We will present results forecasting the magnitude of the statistical device variability in the next technology generations based on comprehensive physical 3D statistical simulation. A methodology for transferring of this information into industry standard compact models like BOSIM4 and BISIMSOI will also be presented. The use of compact models in statistical circuit simulations of inverters and the implications for the supply voltage will also be discussed.



George Constantinides, Imperial College "Low Power Design for Reconfigurable Computing".

In this talk, we will focus on the sources of power consumption in modern reconfigurable logic devices (FPGAs) implementing numerical algorithms. The requirement for early-stage power estimation models for arithmetic circuits will be developed, and the challenges involved will be discussed. Some results from our research indicating the accuracy achievable at various levels of abstraction will be presented. We will close with one suggested use for high-level power models: allowing the automatic optimal tradeoff of power consumption for arithmetic roundoff error.

Steve Beeby, Southampton Uni. 'Vibration Energy Harvesting: Background and state of the art'

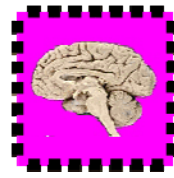
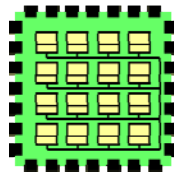
This talk presents an overview of vibration energy harvesting. It describes the basic techniques for converting kinetic energy in the environment into electrical energy. These principles will be demonstrated by various examples designed to convert energy from human motion and industrial vibrations

Roger Woods, Queens Uni. Belfast "The need to mix programmability and low power"

The talk will consider the importance of applying a system-level design emphasis to the creation of complex DSP systems. With increasing system level costs, increasing DSP platforms are being created to be programmable leading to new DSP platforms such as the Storm processor or Picochip hardware platform or heterogeneous platforms such as multiprocessor and/or multi-FPGA. Whilst this can reduce risk, the danger is that power will be sacrificed for this programmable gain. The talk will look at some approaches to reduce power consumption by looking at a suitable system-level platform that the University is developing.

Alex Yakovlev, Newcastle Uni., "From low power computing to power-adaptive computing"

Traditional drive for low power computing has been largely motivated by the fact that the energy resources are limited by the battery. In the realm of the deep-submicron CMOS and "More than Moore" diversification, opportunities are sought outside the customary energy-saving paradigm. In this talk we focus on systems where energy sources need not be necessarily bounded though power may be rationed according to certain design requirements. For example, there can be limits on the allowed heat dissipation on a chip or the system is power-sourced from a harvester with certain power-voltage dynamics. In such cases the power-flow and information-flow should be considered holistically, possibly even at the same level of design abstraction, thereby forming a new class of optimization problems. For example, in the case of energy-harvester-based supply one might want to maximize the computational output bearing in mind different operation modes of the harvester. We would also like to speculate on how future developments of computation electronics can be affected by this paradigm change.



Speaker Bios

Bashir Al Hashimi Southampton University (Project COOrdinator)



Bashir M. Al-Hashimi is Professor of Computer Engineering in the [School of Electronics and Computer Science](#), [University of Southampton](#), a Director of the [Pervasive Systems Centre](#), and Deputy Head of School (Education). His research interests are system-on-chip and embedded computing systems with particular focus on low-power design and low-cost test. He is the Principal Investigator on the EPSRC platform grant on [Electronics Design](#)

Professor Al-Hashimi is the Editor-in-Chief of the [IEE Proceedings: Computer and Digital Techniques](#) and on the editorial board of [Journal of Electronic Testing: Theory and Applications \(JETTA\)](#), [Journal of Embedded Systems](#), and [Journal of Low Power Electronics](#). He is a member of the executive team of the [IEE Microelectronics and Embedded Systems Professional Network](#), [Design, Automation and Test in Europe \(DATE\) conference](#), [European Test Symposium](#) and the [European Workshop on Microelectronics education](#). He was the general chair of the [11th IEEE European Test Symposium](#), and the general chair DATE Friday Workshops (2005, 2006 and 2007). Professor Al-Hashimi published over 180 papers and authored and co-authored 4 books on [circuit simulation](#), [low power design](#) and [test](#). Recently he edited the IEE Press book, [System-on-Chip: Next Generation Electronics](#). Professor Al-Hashimi is a Fellow of the Institution of Engineering and Technology, Fellow of the British Computer Society, and Senior Member of the Institution of Electrical and Electronics Engineers.

Asen Asenov, Glasgow Uni.

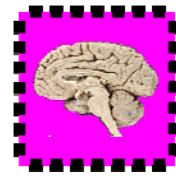
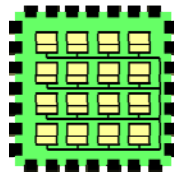
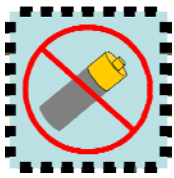


Asen Asenov received his MSc degree in solid state physics from Sofia University, Bulgaria in 1979 and PhD degree in physics from The Bulgarian Academy of Science in 1989. He had 10 years industrial experience as a head of the Process and Device Modelling Group in IME - Sofia, developing one of the first integrated process and device CMOS simulators IMPEDANCE. In 1989-1991 he was a visiting professor at the Physics Department of TU Munich.

He joined the [Department of Electronics and Electrical Engineering](#) at the [University of Glasgow](#) in 1991 and served as a Head of Department in 1999-2003.

As a professor of Device Modelling, leader of the [Device Modelling Group](#) he coordinates the development of 2D and 3D quantum mechanical, Monte Carlo and classical device simulators and their application in the design of advanced and novel CMOS devices. He has pioneered the simulations and the study of various sources of intrinsic parameter fluctuations in decanano and nano CMOS devices including random dopants, interface roughness and line edge roughness.

Dr Asenov is a fellow of the Royal Academy of Scotland, a Senior Member of IEEE and a member of the IEEE EDS TCAD Committee. He is currently a member of the programme committees for IEDM, ESSDERC, IWCE, SNW, HCIS and IEEE Nano Conf, a Program Committee Chair for SNW2006 and Symposium B



organiser at the E-MRS2006 Spring Meeting. He has over 330 publications in process and device modelling and simulation, semiconductor device physics, 'atomistic' effects in ultra-small devices and impact of variations on circuits and systems including in the last 5 years more than 15 papers in IEEE Transaction journals. In the last 5 years he has given also more than 65 invited talks at prestigious international conferences and meetings in Europe, USA and Japan.

George Constantinides, Imperial College



George Constantinides is a Senior Lecturer at Imperial College. He obtained an MEng and PhD from Imperial College in 1998 and 2001, respectively. He is an associate editor of the IEEE Transactions on Computers and the Journal of VLSI Signal Processing. He was Programme Co-Chair of the IEEE International Conference on Field-Programmable Technology (FPT) in 2006 and Field Programmable Logic (FPL) in 2003. He currently serves on the programme committees of five international conferences, including FPL, DATE, ASAP, and FPT, and is Architectural Synthesis Track Chair for DATE 2009. He has published over 90 research papers in peer-refereed journals and international conferences.

He has held two EPSRC grants as PI in the field of reconfigurable hardware, is co-investigator on an EPSRC Plaform Grant supporting the group at Imperial College and is co-investigator on an EPSRC Digital Economy Cluster grant bringing together Oxford, Imperial, Belfast and Manchester to collaborate on hardware accelerator technologies and their applications. Dr Constantinides is a winner of the Eryl Cadwaladar Davies Prize for the best doctoral thesis in Electrical Engineering at Imperial College, and is a joint recipient of an Imperial College Research Excellence Award (2006).

Steve Beeby, Southampton University.



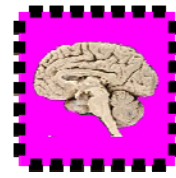
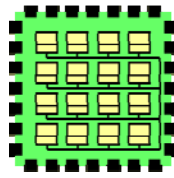
Steve Beeby obtained a PhD from the University of Southampton in 1998 on the subject of micromechanical resonators and was awarded a prestigious EPSRC Advanced Research Fellowship in 2001. He has been involved in energy harvesting for over 10 years and was the project co-ordinator of an EU Framework 6 STREP project 'Vibration Energy Scavenging (VIBES)'. He is a co-founder of Perpetuum Ltd, a University spin-out based upon vibration energy harvesting formed in 2004. He has over 130 publications in the field and 5 patents, and currently he is a Reader in the School of Electronics and Computer Science.

Roger Woods, Queens Uni. Belfast



Roger Woods is a Professor of Digital Systems, leading a team of 14 people in the Programmable Systems Laboratory in Queen's University of Belfast. He has over 20 years of hardware design experience and is internationally recognised for his expertise for implementation of telecommunication and DSP applications. He has considerable experience on working collaboratively with industry and has

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developed a number of chips, some of which have since been used commercially. He was general chair of the Field Programmable (FPL) conference in Belfast (2001), the IEE's FPGA Developer's Forum in 2003 and 2005, the strategy forum of the 1st International Conference on Commercialising Technologies and Innovation conference and the 1st Microelectronics and Embedded Systems conference in Singapore, Jan 2007. He was program chair of the Advanced Reconfigurable Computing conference in 2008 and is on numerous program committees. He has published over 130 scientific papers and holds a number of patents in the real-time implementation of digital filters. He has just authored a book entitled "FPGA-based Implementation of Signal Processing Systems" with Wiley. His research interests include programmable hardware for telecommunications and DSP applications, programmable solutions for programmable hardware applications, design tool flows and methodologies.

Alex Yakovlev, Newcastle Uni.



Alex Yakovlev (DSc) leads the Newcastle Microelectronics Systems Design Group and coordinates the developments of automated design methods for asynchronous circuit design, cryptographic hardware, multi-clock SoCs and NoCs, low-power event processors and variability analysis based on DoE/RSM techniques. He has over 200 publications and several patents on electronic and computer systems design. He is a recognized authority in the area of modelling digital systems and SoC using Petri nets, where he authored and edited several monographs. He is the steering committee chairman of the IEEE ACSD Conference, General chair of IEEE ASYNC'08 and NOC'08 Symposia, TPC member of DATE, ACSD, ATPN, ASYNC, NOCS and other conferences.